What is claimed is:

1. A high voltage generation and regulation circuit, having a plurality of operational phases, for use in a memory device erase operation, the circuit comprising:
a positive high voltage pump that generates a positive high voltage signal for use in the memory device erase operation;
a negative high voltage pump that generates a negative high voltage signal for use in the memory device erase operation; and
an auxiliary voltage generator that generates an auxiliary voltage and a control signal for controlling a rate of discharge of the positive high voltage signal.

2. The circuit of claim 1 and further including:
a first discharge path coupled to the positive high voltage pump and the auxiliary voltage generator, the control signal controlling the rate of discharge of the positive high voltage signal through the first discharge path; and
a second discharge path coupled to the negative high voltage pump and the auxiliary voltage generator, the second discharge path discharging the negative high voltage signal in response to the auxiliary voltage.

3. The circuit of claim 1 wherein the plurality of operational phases comprise an off state, a ramp phase, a pulse state, a slow discharge phase and a fast discharge phase.

4. The circuit of claim 3 wherein the negative high voltage signal drives the auxiliary voltage during the ramp and pulse phases and the auxiliary voltage discharges the negative high voltage signal during at least one discharge phase.

5. The circuit of claim 1 and further including an enable signal, coupled to the auxiliary voltage generator, that at least in part enables/disables the auxiliary voltage generator.

6. The circuit of claim 1 and further including a negative level shifter coupled to the negative high voltage pump that translates an input select signal having a voltage range of 0V to V_{CC} to a high voltage signal having a voltage in the range of the negative high voltage signal as a minimum to V_{CC} as a maximum.

7. The circuit of claim 6 wherein the auxiliary voltage is input to the negative level shifter to reduce transistor drain-source stress in the level shifter

8. A high voltage generation and regulation circuit, having a plurality of operational phases, for use in a memory device erase operation, the circuit comprising:
a positive high voltage pump that generates a positive high voltage signal for use in the memory device erase operation;
a negative high voltage pump that generates a negative high voltage signal for use in the memory device erase operation;
a first discharge path coupled to the positive high voltage pump;
a second discharge path coupled to the negative high voltage pump; and
an auxiliary voltage generator that generates, in response to an enable signal, an auxiliary voltage and a fast discharge control signal for controlling a rate of discharge of the positive high voltage signal through the first discharge path.

9. The circuit of claim 8 and further including a DC control block, coupled between the auxiliary voltage generator and the first discharge path, for selecting the rate of discharge in response to the enable signal and the fast discharge control signal.

10. The circuit of claim 8 and further comprising:
a switch, coupled to the negative high voltage pump, for controlling the output of the negative high voltage signal in response to an address generated select signal; and

a memory sector select switch, coupled to the positive high voltage pump, for controlling to which memory sector of the memory device the positive high voltage signal is coupled in response to the select signal.

11. The circuit of claim 8 and further comprising:

a first on/off control block coupled to the positive high voltage pump for increasing the voltage level of the positive high voltage signal in response to a difference between a reference positive high voltage signal and the positive high voltage signal; and

a second on/off control block coupled to the negative high voltage pump for increasing the voltage level of the negative high voltage signal in response to a difference between a reference negative high voltage signal and the negative high voltage signal.

12. A high voltage generation and regulation circuit, having a plurality of operational phases, for use in a memory device erase operation, the circuit comprising:

a positive high voltage pump that generates a positive high voltage signal for use in the memory device erase operation;

a negative high voltage pump that generates a negative high voltage signal for use in the memory device erase operation;

a first discharge path coupled to the positive high voltage pump;

a second discharge path coupled to the negative high voltage pump;

an auxiliary voltage generator that generates, in response to an enable signal, an auxiliary voltage and a fast discharge control signal; and

a discharge rate control circuit, coupled between the auxiliary voltage generator and the first discharge path, for selecting, in response to the enable signal and the fast discharge control signal, a fast discharge rate or a slow discharge rate of the positive high voltage signal through the first discharge path.

13. The circuit of claim 12 and further including:

a negative level shifter coupled to a memory address generated select signal, the negative high voltage signal, and the auxiliary voltage for reducing transistor drain-source stress, the negative level shifter outputting the negative high voltage signal in response to the select signal; and

an insulated NMOS switch, coupled to the negative high voltage pump and the negative level shifter, for disabling output of the negative high voltage signal to the memory device in response to the negative high voltage signal from the negative level shifter.

14. The circuit of claim 13 and further including a sector selector, coupled to the positive high voltage signal, for controlling output of the positive high voltage signal to memory cells of the memory device in response to the select signal.

15. An electronic system comprising:

a processor that generates memory control signals; and

a memory device, coupled to the processor, for storing and erasing data in response to the memory control signals, the memory device comprising memory cells for storing the data and a high voltage generation and regulation circuit, having a plurality of operational phases, for use in an erase operation, the circuit comprising:

a positive high voltage pump that generates a positive high voltage signal for use in the erase operation;

a negative high voltage pump that generates a negative high voltage signal for use in the erase operation; and

an auxiliary voltage generator that generates an auxiliary voltage and a control signal for controlling a rate of discharge of the positive high voltage signal.

16. The electronic system of claim 15 wherein the memory device is a NAND flash memory.

17. The electronic system of claim 15 wherein the memory device is a NOR flash memory.

18. A voltage generator for generating an auxiliary voltage for use in a high voltage generation and regulation circuit having a negative high voltage pump that generates a negative high voltage, a positive high voltage pump that generates a positive high voltage, an enable signal that enables the generation of the negative and positive high voltages, and a plurality of discharge paths, each coupled to a different voltage pump, the discharge paths experiencing either a fast or a slow discharge phase, the voltage generator comprising:

output control logic that controls output of a discharge rate control signal;

a plurality of NMOS transistors coupled together serially in a diode-like fashion, one end of the plurality of NMOS transistors coupled to and discharging the negative high voltage when the plurality of NMOS transistors are turned on;

a low voltage enabling transistor, coupled to the enable signal, for enabling the voltage generator in response to the enable signal;

a first high voltage insulating transistor, coupled between the low voltage enabling transistor and the plurality of NMOS transistors, a node formed at the junction of the first high voltage insulating transistor and a remaining end of the plurality of NMOS transistors having a voltage that rises in response to the low voltage enabling transistor being turned on;

a first high voltage enabling transistor coupled between V_{CC} and the node, a control gate of the first high voltage enabling transistor coupled to an output of the output control logic, the first high voltage enabling transistor being turned on in response to the discharge rate control signal;

a second high voltage insulating transistor coupled between the node and the output control logic, a control gate of the second high voltage insulating transistor coupled between two of the plurality of NMOS transistors; and

a second high voltage enabling transistor coupled between V_{CC} and the auxiliary voltage output, a control gate of the second high voltage enabling transistor coupled to the output of the output control logic, the second high voltage enabling transistor being turned on in response to the discharge rate control signal and generating the auxiliary voltage.

19. The voltage generator of claim 18 wherein the output control logic comprises:
a high voltage inverter having an input coupled to the first high voltage insulating transistor;
a first low voltage inverter coupled to an output of the high voltage inverter;
a NAND gate having a first input coupled to the low voltage inverter and a second input coupled to the enable signal; and
a second inverter coupled to an output of the NAND gate.

20. A method for generating erase voltages for a memory device, the method comprising:
generating a positive high voltage signal in response to an enable signal;
generating a negative high voltage signal in response to the enable signal;
generating an auxiliary voltage signal and a fast discharge control signal in response to the enable signal;
discharging the positive high voltage signal at a slow discharge rate in response to a state of the fast discharge control signal; and
discharging the positive high voltage signal at a fast discharge rate in response to the state of the fast discharge control signal.

21. The method of claim 19 and further including applying the auxiliary voltage signal to a negative level shifting circuit to reduce drain-source stress on transistors that are off.

22. The method of claim 20 and further including applying the positive high voltage signal and the negative high voltage signal to a plurality of memory cells of the memory device.

23. A memory device comprising:
memory cells for storing the data; and
a high voltage generation and regulation circuit, having a plurality of operational phases, for use in an erase operation of the memory cells, the circuit comprising:
a positive high voltage pump that generates a positive high voltage signal for use in the erase operation;
a negative high voltage pump that generates a negative high voltage signal for use in the erase operation; and
an auxiliary voltage generator that generates an auxiliary voltage and a control signal for controlling a rate of discharge of the positive high voltage signal.

24. The memory device of claim 23 wherein the high voltage generation and regulation circuit further comprises a negative level shifting circuit, coupled to the auxiliary voltage, such that the auxiliary voltage reduces drain-source stress of transistors in the negative level shifting circuit that are in an off state.